WHAT IS CLAIMED IS:

1. A system timer for controlling the timing at which a communication device communicates, said system timer comprising:

a memory device adapted to store a set of software instructions;

a processor coupled to said memory device, said processor being adapted to execute any of said software instructions in any of a plurality of sequences, each of said sequences causing said processor to generate a corresponding set of control signals, each of said corresponding set of control signals being adapted to enable communication by said communication device in one of a multiplicity of communication formats, wherein each of said communication formats defines the timing at which a set of data is communicated by said communication device.

2. The system timer of claim 1 wherein said processor comprises a first processor and further wherein said communication device comprises a second processor, wherein said plurality of sequences in which said first processor executes said software instructions is controlled by said second processor.

3. The system timer of claim 2 wherein said system timer further comprises a memory register for storing addresses, said addresses indicating a set of locations at which at least some of said software instructions are stored in said memory device, wherein said first processor is adapted to extract said addresses from said memory register and to execute said software instructions located at said addresses thereby causing said first processor to execute said software instructions in a sequence defined by an order in which said addresses are stored in said memory register.

4. The system timer of claim 3 wherein said second processor controls said plurality of sequences in which said first processor executes said software instructions by controlling said order in which said addresses are stored in said memory register.

5. The system timer of claim 4 wherein said software instructions comprise a first software instruction that, when executed by said first processor, causes said first processor to extract one of said addresses stored in said memory register and to execute a second software instruction located at said one of said addresses provided that said second processor has caused at least one of said addresses to be stored in said memory register.

6. The system timer of claim 5 wherein said first software instruction further causes said first processor to execute a third software instruction stored in said memory device provided that said second processor has not stored said at least one address in said memory register, wherein an address at which said third software instruction is stored in said memory device is specified in said first software instruction.

7. The system timer of claim 2 wherein said set of software instructions stored in said memory device comprises a first instruction, said first instruction, when executed by said first processor, causing said first processor to execute a first sequence of software instructions provided that a condition has been satisfied by said second processor and further causing said first processor to execute a second sequence of software instructions provided that said condition has not been satisfied.

8. The system timer of claim 7 wherein said first sequence of software instructions begins with a second instruction located at an address specified in said first instruction.

9. The system timer of claim 7 wherein said condition comprises a mode bit being set to a first logic level.

10. The system timer of claim 7 wherein said condition comprises an equation being equal to a predefined value.

11. The system timer of claim 10 wherein said equation being equal to said predefined value depends upon whether a set of mode bits have been set by said second processor.

12. The system timer of claim 2 wherein said plurality of sequences comprises a first sequence that causes said communication device to perform single slot communication and wherein said second processor is adapted to modify said first sequence to a second sequence that causes said communication device to perform multi-slot communication.

13. The system timer of claim 2 wherein said second processor controls said sequence by setting a control bit stored in a memory register.

14. The system timer of claim 2 wherein said second processor comprises a digital signal processor.

15. The system timer of claim 2 wherein said second processor comprises a microprocessor.

16. The system timer of claim 1 wherein said plurality of sequences comprises a first sequence of said software instructions that, when executed by said first processor, enables operation of said communication device in a first mode, wherein said plurality of sequences further comprises a second sequence of said software instructions that, when executed by said first processor, enables operation of said communication device in a second mode, and wherein said second processor is adapted to cause said first processor to switch between executing said first and second sequences thereby causing said communication device to switch between said first and second modes.

17. The system timer of claim 16 wherein said first mode comprises a stand by mode and wherein said second mode comprises an acquisition mode.

18. The system timer of claim 16 wherein said first mode comprises an acquisition mode and wherein said second mode comprises a steady state mode.

19. The system timer of claim 1 wherein said multiplicity of communication formats comprises a single slot communication format.

20. The system timer of claim 1 wherein said multiplicity of communication formats comprises a multi-slot communication format.

21. A system timer for controlling a timing at which a set of data frames are communicated between a first communication device and a second communication device, wherein said system timer is disposed in said first communication device, said system timer comprising:

a processor adapted to adjust a frame length during which a first

frame of data is communicated, wherein adjusting said frame length of said first frame of data causes a start time of a second frame of data to be adjusted and further wherein adjusting said start time of said second frame of data causes a communication time slot to be adjusted, said communication time slot occurring at a fixed start time relative to said start time of said second frame of data.

22. The system timer of claim 21 wherein said frame length comprises a first frame length, said system timer further comprising:

a counter adapted to count at a rate that corresponds to a set of clock pulses and further being adapted to wrap to zero upon reaching said first frame length;

a first memory register for storing said first frame length;

a second memory register for storing a second frame length;

said processor being adapted to adjust said first frame length by causing said counter to wrap to zero upon reaching said second frame length.

23. The system timer of claim 22 wherein said communication time slot comprises a first communication time slot and further wherein said processor is further adapted to adjust said counter by an amount of time equal to an offset value upon executing a software instruction thereby causing a time at which a second communication time slot occurs to be adjusted by said amount of time equal to said offset value.

24. The system timer of claim 23 wherein said software instruction includes a field for containing data that indicates whether said counter will be incremented by said offset value.

25. The system timer of claim 23 wherein said software instruction includes a field for containing data that indicates whether said counter will be decremented by said offset value.

26. The system timer of claim 23 wherein said offset value is equal to an amount of time by which the timing of the first communication device is offset from the timing of the second communication device.

27. The system timer of claim 23 further comprising a memory device for storing said software instruction.

28. The system timer of claim 23 wherein said first communication time slot comprises a receive time slot during which said first communication device is configured to receive data and wherein said second communication time slot comprises a transmit time slot during which said first communication device is configured to transmit data.

29. A system timer for controlling a timing at which a set of data frames having a set of time slots are communicated between a first communication device and a second communication device, wherein said system timer is disposed in said first communication device, said system timer comprising:

a processor adapted to adjust a first time slot in a first direction to compensate for a first timing offset, said processor being further adapted to adjust a second time slot in a second direction to compensate for a second timing offset, wherein said first time slot occurs in each of said frames before said second time slot, and further wherein said processor adjusts said second

time slot after said first time slot has ended.

30. The system timer of claim 29 wherein said first time slot is fixed relative to a frame start and wherein said processor is adapted to adjust said first time slot in said first direction by adjusting said frame start in said first direction.

31. The system timer of claim 30 wherein said frame start is associated with a first frame and wherein said processor is adapted to adjust said frame start in said first direction by adjusting a frame length of a second frame, said second frame preceding said first frame.

32. The system timer of claim 31 further comprising a memory register for storing a frame length value and a counter associated with said timing at which said frames are communicated, said counter being adapted to wrap to zero upon reaching said frame length value, wherein said processor is adapted to adjust said frame length of said second frame by changing said frame length value during said second frame.

33. The system timer of claim 29 further comprising a counter associated with said timing at which said frames are communicated, wherein said processor adjusts said second time slot in said second direction by causing said counter to be adjusted.

34. The system timer of claim 29 wherein adjusting said first time slot in said first direction causes said first time slot to occur later and wherein said step of adjusting said second time slot in said second direction causes said second time slot to occur earlier.

35. The system timer of claim 34 wherein said first time slot comprises a receive slot during which said first communication device is configured to receive data from said second communication device and wherein said second time slot comprises a transmit slot during which said first communication device is configured to transmit data to said second communication device.

36. The system timer of claim 34 wherein said receive slot is adjusted to occur later so that said data transmitted by said second communication device has sufficient time to reach said first communication device and wherein said transmit slot is adjusted to occur earlier so that said data transmitted by said first communication device has sufficient time to reach said second communication device.

37. A method for controlling the timing at which a communication device communicates, said communication device comprising a first processor and a system timer, said system timer comprising a second processor and a memory device adapted to store a set of software instructions, said method comprising the steps of:

causing said second processor to execute a set of software instructions in any of a plurality of sequences, each of said sequences causing said second processor to generate a corresponding set of control signals, each of said corresponding set of control signals being adapted to enable communication by said communication device in one of a multiplicity of communication formats, wherein each of said communication formats defines the timing at which a set of data is communicated by said communication device; and,

causing said first processor to define said sequences in which said second processor executes said software instructions.

38. The method of claim 37 wherein a first of said sequences causes said communication device to communicate in a first timing format and wherein a second of said sequences causes said communication device to communicate in a second timing format.

39. The method of claim 37 wherein said first timing format comprises a single slot timing format and wherein said second timing format comprises a multi-slot timing format.

40. The method of claim 37 wherein a first of said sequences defined by said first processor causes said communication device to operate in a first mode and wherein a second of said sequences defined by said first processor causes said communication device to communicate in a second mode.

41. The method of claim 39 wherein said first mode comprises a stand by mode and wherein said second mode comprises an acquisition mode.

42. The method of claim 40 wherein said first mode comprises an acquisition mode and wherein said second mode comprises a steady state mode.

43. The method of claim 36 wherein said first processor defines said sequences in which said second processor executes said software instructions by storing a set of addresses in an order in a memory register disposed in said system timer, said set of addresses indicating a set of locations at which at least some of said software instructions are stored in said memory device, wherein said second processor is adapted to extract and execute said addresses from said memory register in said order in which said addresses are stored.

44. The method of claim 36 wherein an order in which said instructions are executed in at least one of said sequences is dependent upon said first processor setting a mode bit to a first logic level.

45. A method for compensating for a first timing offset associated with a first time slot and for compensating for a second timing offset associated with a second time slot, said first time slot and said second time slot occurring in each of a set of frames, wherein said first time slot occurs before said second time slot, said method comprising the steps of:

adjusting said first time slot in a first direction during a first frame, said first time slot being fixed relative to a frame start associated with said first frame, wherein said first time slot is adjusted in said first direction by adjusting said frame start associated with said first frame in said first direction; and,

adjusting said second time slot in a second direction after said first time slot has ended.

46. The method claim 45 wherein said step of adjusting said first time slot in a first direction during a first frame is performed by adjusting a frame length associated with a second frame, said second frame preceding said first frame.

47. The method of claim 46 wherein said step of adjusting said frame length associated with said second frame is performed by changing a value at which a counter wraps to zero during said second frame.

48. The method of claim 45 wherein said step of adjusting said second time slot in a second direction after said first time slot has ended is performed by causing a counter to be adjusted.

49. The method of claim 45 wherein said step of adjusting said first time slot in said first direction causes said first time slot to occur later and wherein said step of adjusting said second time slot in said second direction causes said second time slot to occur earlier.

50. The method of claim 44 wherein said first time slot comprises a receive slot during which a first communication device is configured to receive a first set of data from a second communication device and wherein said second time slot comprises a transmit slot during which said first communication device is configured to transmit a second set of data to said second communication device.

51. The method of claim 49 wherein said first time slot is adjusted to occur later so that said first set of data has sufficient time to reach said first communication device

52. The method of claim 49 wherein said second time slot is adjusted to occur earlier so that said second set of data has sufficient time to reach said second communication device.